REMARKS

Claims 1-5, and 7-28 are pending in the present application. Claim 6 was canceled; and claims 1, 8, 15, 19-20, 22, and 26-27 were amended. Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102, Anticipation, Claims 8-14, 20-21, and 27-28

The Examiner has rejected claims 8-14, 20-21, and 27-28 under 35 U.S.C. § 102 as being anticipated by *Anderson et al* (US Patent No. 6,338,119). This rejection is respectfully traversed.

With regard to claims 8, 20, and 27, the Examiner states:

> As for claims 8, 20, and 27, Anderson teaches a method of providing data to an I/O adapter from a bus bridge (see figure 1, bus bridge 108, I/O devices 118, 120 and column 5 lines 8-11, wherein the bus bridge 108 are transferring data to the I/o devices 118, 120 via a conventional adapter), the method comprising:
>
> receiving a request for data from the I/O adapter (see figure 1, bridge 108 and column 7 lines 8-10 and column 7 lines 45-49, wherein figure 1 discloses I/O devices 118, 120 which are communicating with symmetric multi-processors (SMP) 102 via bridge 108 and conventional adapter and vice versa for the SMP to communicate with the I/O devices 118, 120. Further, bridge 108 maintains cache 108 coherency as cited in column 4 lines 63-67);
>
> responsive to a determination that the requested data is contained within a cached memory (see figure 1, cache 109), providing the requested data using the data in the cached memory (see figure 1, PCI host bridge 108, cache 109, figure 4 step 406 and 7 lines 6-10, wherein the PCI host bridge determined whether cache 109 is valid or invalid).

(*Office Action*, dated April 8, 2003, pages 2-3).

A prior art reference anticipates the claimed invention under 35 U.S.C. §102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). *Anderson* cited by the Examiner does not anticipate the present invention as recited in amended claim 8, because *Anderson* fails to teach each and every element of the amended claim. Amended independent claim 8, which is representative of amended independent claims 20 and 27, reads as follows:

8. A method of providing data to an I/O adapter from a peripheral component interconnect to peripheral component interconnect bridge, the method comprising:

receiving a request for data from the I/O adapter;

responsive to a determination that the requested data is contained in a cached memory within the peripheral component interconnect to peripheral component interconnect bridge, providing the requested data using the data in the cached memory.

Claim 8 in its amended form recites a method of providing data to an I/O adapter from a peripheral component interconnect (PCI) to peripheral component interconnect (PCI) bridge. Claim 8 recites the feature of providing requested data using the data in the cached memory within the PCI to PCI bridge. Cache memory **220** and **226** are located within PCI to PCI bridges **216** and **222**, as shown in Figure 2 and in the following cited sections of the Specification:

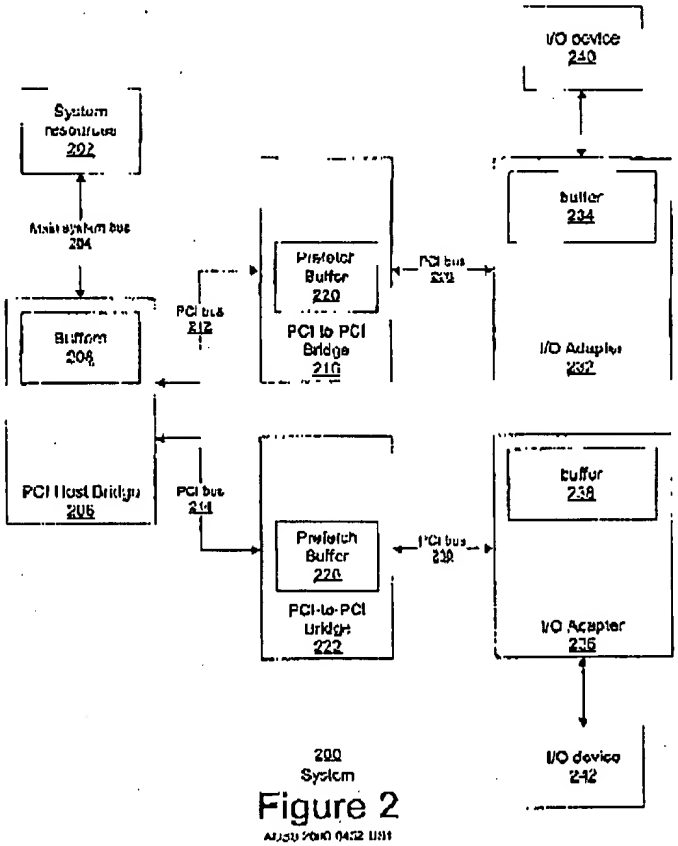

Figure 2

> With reference now to **Figure 2**, a block diagram illustrating PCI host bridge and PCI-to-PCI bridge system is depicted in accordance with the present invention. System **200** may be implemented as data processing system **100** in **Figure 1**. System **200** shows, in greater detail, the functioning of a PCI host bridge, PCI-to-PCI bridge, and I/O adapter system within a data processing system, such as, for example, data processing system **100** in **Figure 1**.

(*Specification*, page 8, line 27 to page 9, line 5).

> When one of I/O devices **240** and **242** requests data, this request is sent through I/O adapters **232** and **236** to its respective PCI-to-PCI Bridge **216** and **222**. The respective one of PCI-to-PCI Bridges **216** and **222** prefetches the data from system resources **202** and caches (stores) the data in its prefetch buffer **220** and **226**. The data is then sent to the respective I/O adapter **232** and **236** which stores the data in its respective buffer **234** and **238**. The respective buffers **234** and **238** may not be able to store the same amount of data as the respective one of prefetch buffers **220** and **226**. However, since the data is cached in a respective one of prefetch buffers **220** and **226**, when the respective one of I/O adapters **232** and **236** is ready for the next portion of the requested data, rather than refetching the data from the system resources, the respective one of prefetch buffers **216** and **222** may simply retrieve the next portion of the requested data from the prefetch buffer **220** and **226** and send the data to the respective one of I/O adapters **232** and **236**. Thus, unnecessary traffic on the main system bus **204** is avoided. Furthermore, the performance of the PCI-to-PCI bridges **216** and **222** are also improved since thrashing on the PCI buses **212** and **214** is reduced.

(*Specification*, page 9, line 25 to page 10, line 17).

As is shown above, the present invention employs prefetch buffers **220** and **226** within PCI to PCI bridges **216** and **222**. The present invention also employs a buffer **208** within PCI host bridge **206**. Caching the data in the PCI to PCI bridge reduces the amount of fetching data over and over again from the PCI host bridge buffer which generates a great deal of wasted traffic on the system I/O bus, thus slowing down the performance of the server.

In contrast, Anderson teaches using cache memory in the PCI host bridge and using large on-chip cache (L1) and larger off-chip (L2) cache, as illustrated in Figure 1:

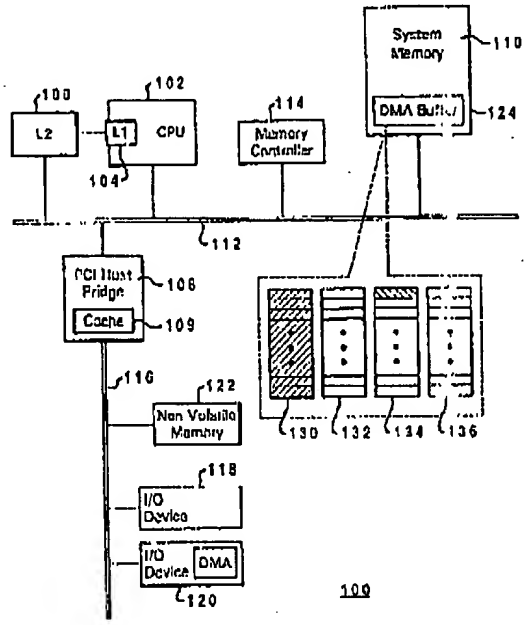

Fig. 1

Figure 1 of the Anderson reference shows cache **109** and L1/L2 cache **104** and **106**. However, as evident from the illustration, cache **109** is not present within a PCI to PCI bridge as recited in claim 8, but rather cache **109** is located within PCI host bridge **108**.

Likewise, L1/L2 cache is not present within a PCI to PCI bridge as the Specification in *Anderson* discloses:

> Processor 102 includes a level one (L1) cache 104. In order to minimize data access latency, one or more additional levels of cache memory may be implemented within data processing system 100, such as a level two (L2) cache 106.

(*Anderson*, col. 4, lines 12-16).

> L2 cache 106 is a dedicated cache connected between CPU 102 and system memory 110 (via system bus 112).

(*Anderson*, col. 4, lines 35-36). As shown above, the L1/L2 cache is not located within the PCI to PCI bridge. Thus, since there is no teaching in *Anderson* of having a cache memory within a PCI to PCI bridge, the *Anderson* reference fails to teach the feature of

providing requested data using the data in the cached memory within the PCI to PCI bridge as recited in claim 8.

With regard to claim 10, the Examiner states:

> As for claim 10, Anderson teaches a peripheral component interconnect to peripheral component interconnect bridge (see figure 1, I/O devices 118, 120, conventional adapter and column 5 lines, 1-11, wherein I/O devices 118, 120 are connected to conventional adapter i.e. bridge), comprising:
> an interface for sending an receiving data from a PCI host bridge (see figure 1, PCI host bridge 108 and column 5 lines 1-12, wherein data communication are transferring between system memory 110 and I/O devices 118, 120 via PCI host bridge 108 and conventional adapter);
> an interface for sending and receiving data from an input/output adapter (see figure 1, PCI host bridge 108 and column 5 lines 1-12, wherein data communication are transferring between system memory 110 and I/O devices 118, 120 via PCI host bridge 108 and conventional adapter);
> buffers for storing data (see cache 109, system memory 110);
> an interface for receiving signals from the PCI host bridge indicating whether data in the buffers are stale (see figure 4, step 406 and column 7 lines 8-22, wherein the PCI host bridge determines whether cache 109 is invalid i.e. stale); and
> logic for clearing stale data from the buffers and retrieving fresh data from the PCI host bridge (see column 4 lines 63-67 and column 5 lines 27-33, wherein one of the embodiment, Anderson teaches the PCI host bridge maintains cache coherency across L1/L2 caches and cache 109 by clearing buffer memory in cache 109 to make room for new data).

(*Office Action*, pages 3-4). Independent claim 10 reads as follows:

> 10. A peripheral component interconnect to peripheral component interconnect bridge, comprising:
> an interface for sending and receiving data from a PCI host bridge;
> an interface for sending and receiving data from an input/output adapter;
> buffers for storing data;
> an interface for receiving signals from the PCI host bridge indicating whether data in the buffers are stale; and
> logic for clearing stale data from the buffers and retrieving fresh data from the PCI host bridge.

Claim 10 recites the feature of a PCI to PCI bridge comprising buffers for storing data. The Examiner argues that *Anderson* teaches this feature by again pointing to Figure 1, illustrated above. The Examiner states, "cache **109**" and "system memory **110**" in

Figure 1 are "buffers for storing data" (*Office Action*, page 4). However, amended claim 10 does not merely disclose having buffers in general, but instead recites having the buffers for storing data located within the PCI to PCI bridge. In contrast, the buffers shown in Figure 1 are not located within the PCI to PCI bridge. Cache **109** is present within PCI host bridge **108**, and system memory is located on system bus **112**. Thus, as evident from the illustration in Figure 1, cache **109** and system memory **110** are not present within the PCI to PCI bridge. Although *Anderson* separately discloses a 'PCI to PCI bridge' and a 'buffer for storing data', *Anderson* makes no mention of having a buffer within the PCI to PCI bridge. Consequently, *Anderson* fails to teach the feature of a PCI to PCI bridge comprising buffers for storing data, as recited in claim 10.

If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Dependent claims 9, 11-14, 21, and 28 depend from independent claims 8, 10, 20, and 27, respectively. Applicants have already demonstrated claims 8, 10, 20, and 27 to be in condition for allowance. Applicants respectfully submit that claims 9, 11-14, 21, and 28 are also allowable, at least by virtue of their dependency on allowable claims.

Consequently, it is respectfully urged that the rejection of claims 8-14, 20-21, and 27-28 has been overcome.

II. 35 U.S.C. § 103, Obviousness, Claims 1-7, 15-19, and 22-26

The Examiner has rejected claims 1-7, 15-19, and 22-26 under 35 U.S.C. § 103 as being unpatentable over *Anderson* in view of *Anderson et al* (US Patent No. 4,868,783), referred hereinafter as "*Anderson#2*." This rejection is respectfully traversed.

35 U.S.C. § 103(c), effective November 29, 1999, reads as follows:

> (c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Applicants respectfully submit that the present application and *Anderson* were, at the time the invention of the present application was made, commonly owned by

International Business Machines Corporation. *See* 1241 O.G. 97 (December 26, 2000), which states that an Applicant or Applicant's attorney may, pursuant to 35 U.S.C. §103(c), overcome a rejection by making a conspicuous statement that the application under examination and cited reference were commonly owned at the time the invention of the application under examination was made.

Thus, under 35 U.S.C. § 103(c), *Anderson* may not be used as a reference under 35 U.S.C. §103 to reject the claims of the present application. *See* MPEP § 2146.

Therefore, the rejection of claims 1-7, 15-19, and 22-26 under 35 U.S.C. § 103 has been overcome.

III. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 6-30-3

Respectfully submitted,

Cathrine K. Kinslow
Reg. No. 34,285
Carstens, Yee & Cahoon, LLP
P.O. Box 802334
Dallas, TX 75380
(972) 367-2001
Attorney for Applicant